



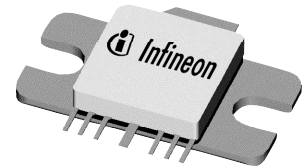
PTMA210452EL
PTMA210452FL
green
Product

Wideband RF LDMOS Integrated Power Amplifier 45 W, 1900 – 2200 MHz

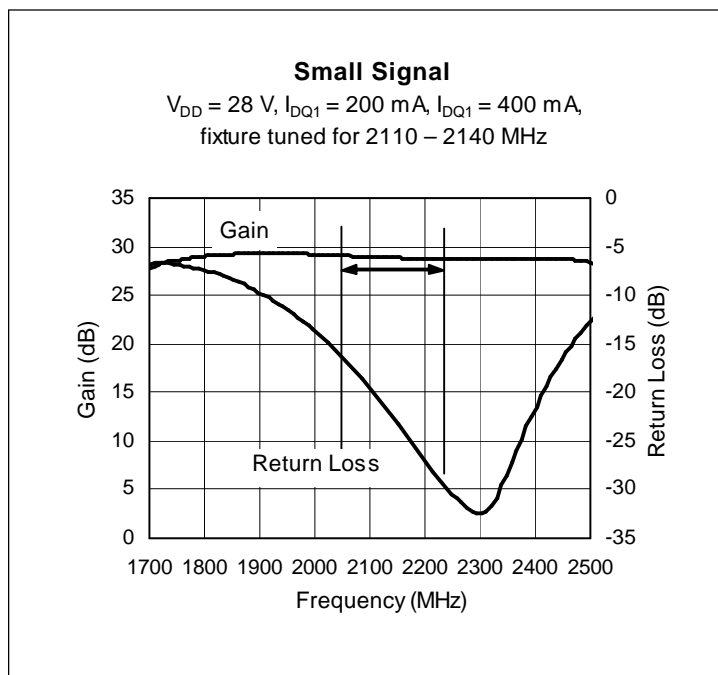
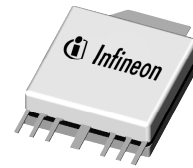
Description

The PTMA210452EL and PTMA210452FL are matched, wideband, 45-watt, 2-stage, LDMOS integrated amplifiers intended for use in all typical modulation formats from 1900 to 2200 MHz. These devices are offered in thermally-enhanced ceramic packages with less than 0.25 micron (10 microinch) gold plating for cool and reliable operation.

PTMA210452EL
Package H-33265-8



PTMA210452FL
Package H-34265-8



Features

- Designed for wide RF and modulation bandwidths and low memory effects
- On-chip matching, integrated input DC block, 50-ohm input and > 5-ohm output
- Typical two-carrier WCDMA performance at 2140 MHz, 28 V
 - Average output power = 3.2 W
 - Linear Gain = 28 dB
 - Efficiency = 10.5%
 - IMD3 = -47 dBc
- Typical two-tone performance, 2140 MHz, 28 V
 - Output power (PEP) = 45 W at IM3 = -30 dBc
 - Efficiency = 32%
- Capable of handling 3:1 VSWR @ 28 V, 45 W (CW) output power
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- High-performance, thermally-enhanced packages, Pb-free and RoHS compliant, with solder-friendly plating

All published data at $T_{CASE} = 25^{\circ}\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

Target RF Characteristics

Two-carrier WCDMA Measurements (tested in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ1} = 200\text{ mA}$ (tuned for linearity), $I_{DQ2} = 450\text{ mA}$ (tuned for linearity & efficiency), $P_{OUT} = 3.2\text{ W}$ average, $f_1 = 2135\text{ MHz}$, $f_2 = 2145\text{ MHz}$, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8 dB @ 0.01% CCDF

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------|------|------|-----|------|
| Input Return Loss | IRL | — | -16 | -10 | dB |
| Gain | G_{ps} | 26.5 | 28 | — | dB |
| Drain Efficiency | η_D | 9 | 10.5 | — | % |
| Intermodulation Distortion, 2-channel WCDMA | IMD | -43 | -47 | — | dBc |

Small-signal CW Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ1} = 200\text{ mA}$, $I_{DQ2} = 450\text{ mA}$, $P_{OUT} = 1\text{ W}$, $f = 2140\text{ MHz}$

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|-----------------|-----------------------|------------|-----|------|-----|----------|
| Gain Flatness | 1 W / 30 MHz | ΔG | — | 0.10 | 0.5 | dB |
| Phase Linearity | | — | -1 | +0.6 | +1 | °/60 MHz |
| Group Delay | $f = 2140\text{ MHz}$ | td | — | 2.16 | — | ns |

DC Characteristics

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---------------------------------|---|---------------|-----|------|------|---------------|
| Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$ | $V_{(BR)DSS}$ | 65 | — | — | V |
| Drain Leakage Current | $V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$ | I_{DSS} | — | — | 1.0 | μA |
| | $V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$ | I_{DSS} | — | — | 10.0 | μA |
| Final Stage On-state Resistance | $V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$ | $R_{DS(on)1}$ | — | 3.5 | — | Ω |
| | | $R_{DS(on)2}$ | — | 0.56 | — | Ω |
| Operating Gate Voltage | $V_{DS} = 28\text{ V}$, $I_{DQ1} = 200\text{ mA}$, $I_{DQ2} = 450\text{ mA}$ | V_{GS} | 2.0 | 2.5 | 3.0 | V |
| Gate Leakage Current | $V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$ | I_{GSS} | — | — | 1.0 | μA |

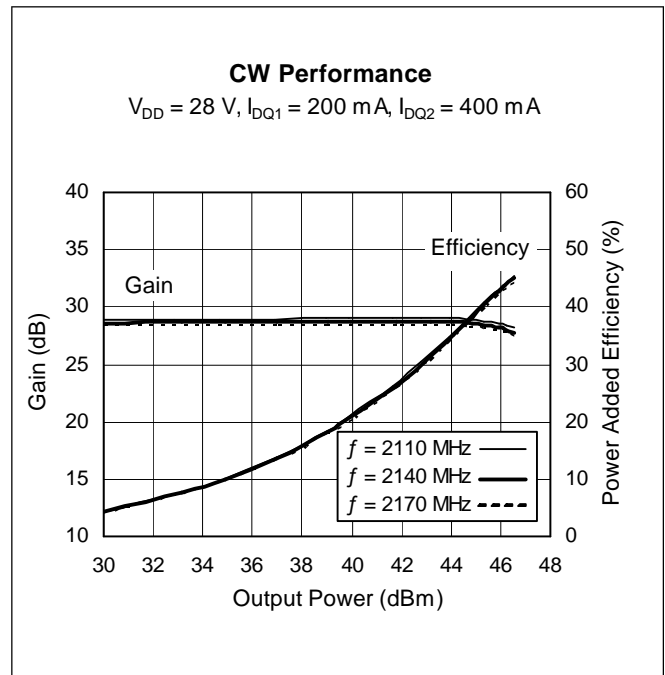
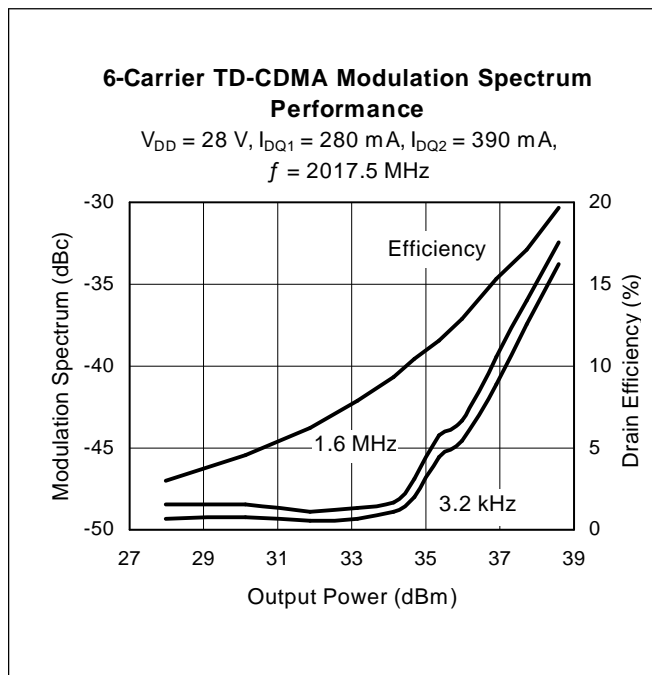
Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-----------------|-------------|------|
| Drain-Source Voltage | V_{DSS} | 65 | V |
| Gate-Source Voltage | V_{GS} | -0.5 to +12 | V |
| Junction Temperature | T_J | 200 | °C |
| Input Power | P_{IN} | 25 | dBm |
| Total Device Dissipation | P_D | 135 | W |
| Above 25°C derate by | | 0.8 | W/°C |
| Storage Temperature Range | T_{STG} | -40 to +150 | °C |
| Thermal Resistance ($T_{CASE} = 70^\circ\text{C}$) Stage 1 | $R_{\theta JC}$ | 3.5 | °C/W |
| Stage 2 | $R_{\theta JC}$ | 1.3 | °C/W |

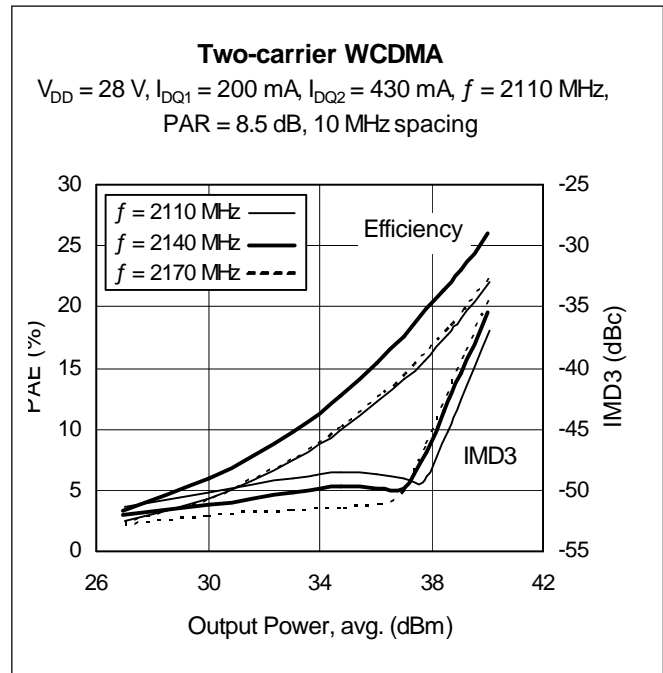
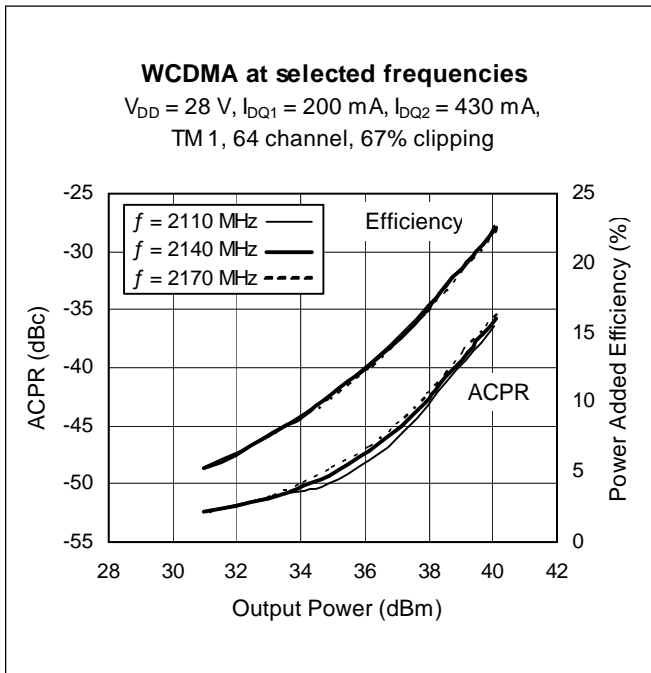
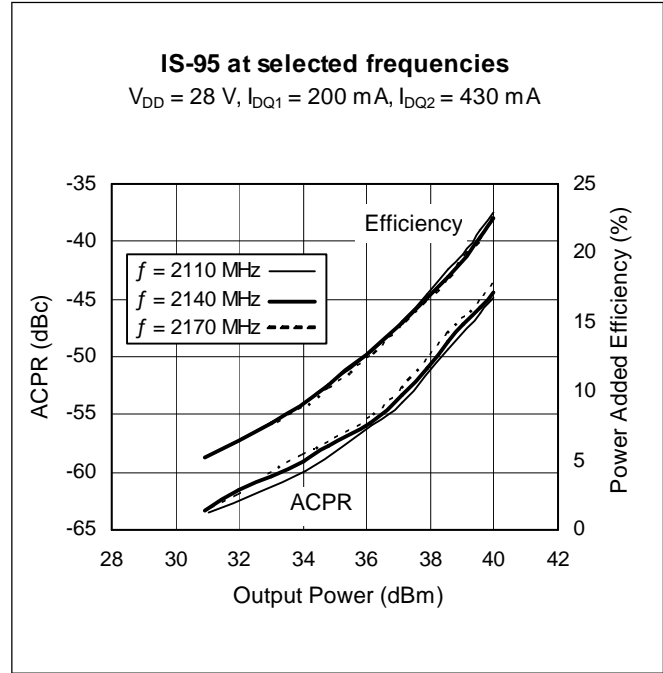
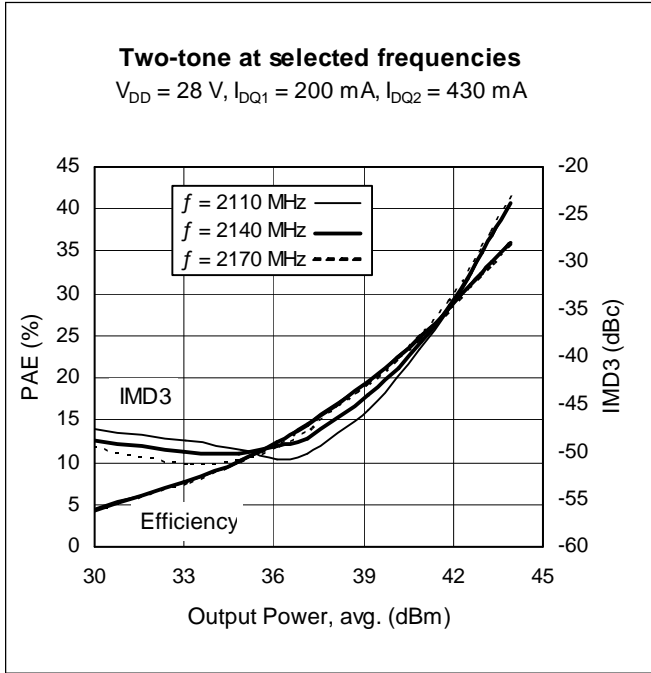
Ordering Information

| Type and Version | Package Outline | Package Description | Shipping | Marking |
|------------------|-----------------|-----------------------------------|----------|--------------|
| PTMA210452EL V1 | H-33265-8 | Thermally-enhanced slotted flange | Tray | PTMA210452EL |
| PTMA210452FL V1 | H-34265-8 | Thermally-enhanced earless flange | Tray | PTMA210452FL |

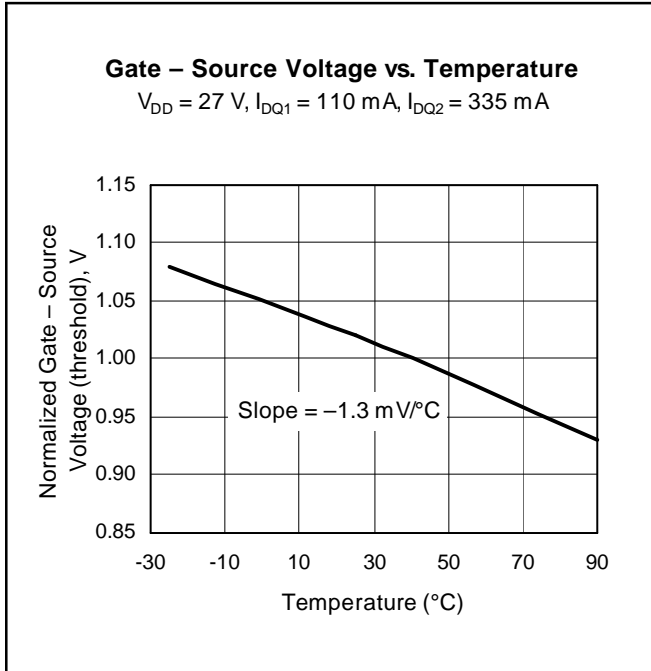
Typical Performance (data taken in a production test fixture)



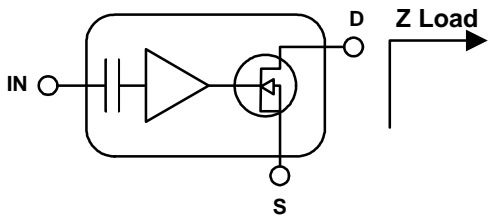
Typical Performance (cont.)



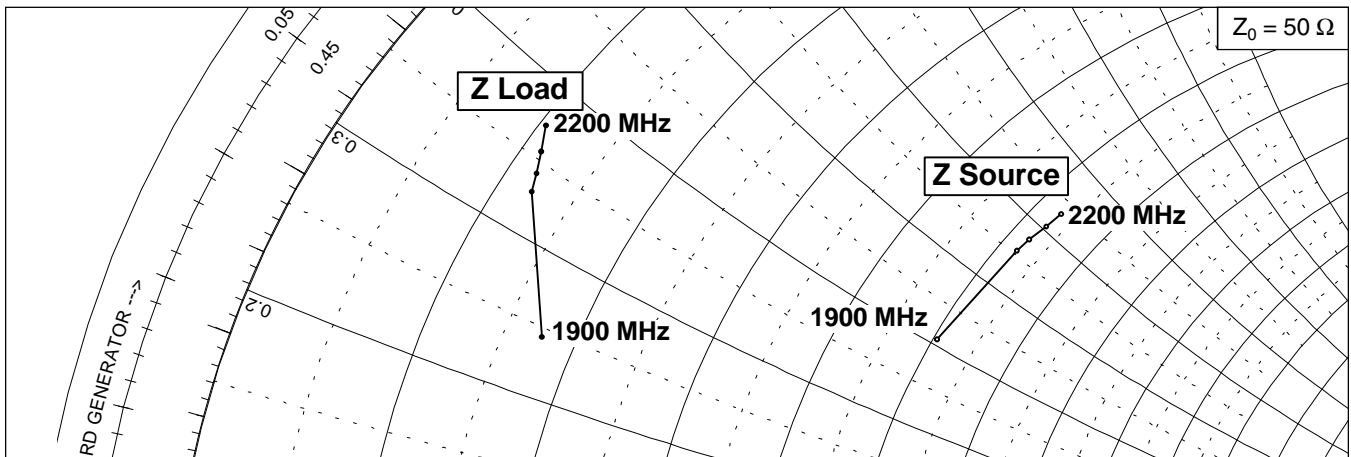
Typical Performance (cont.)



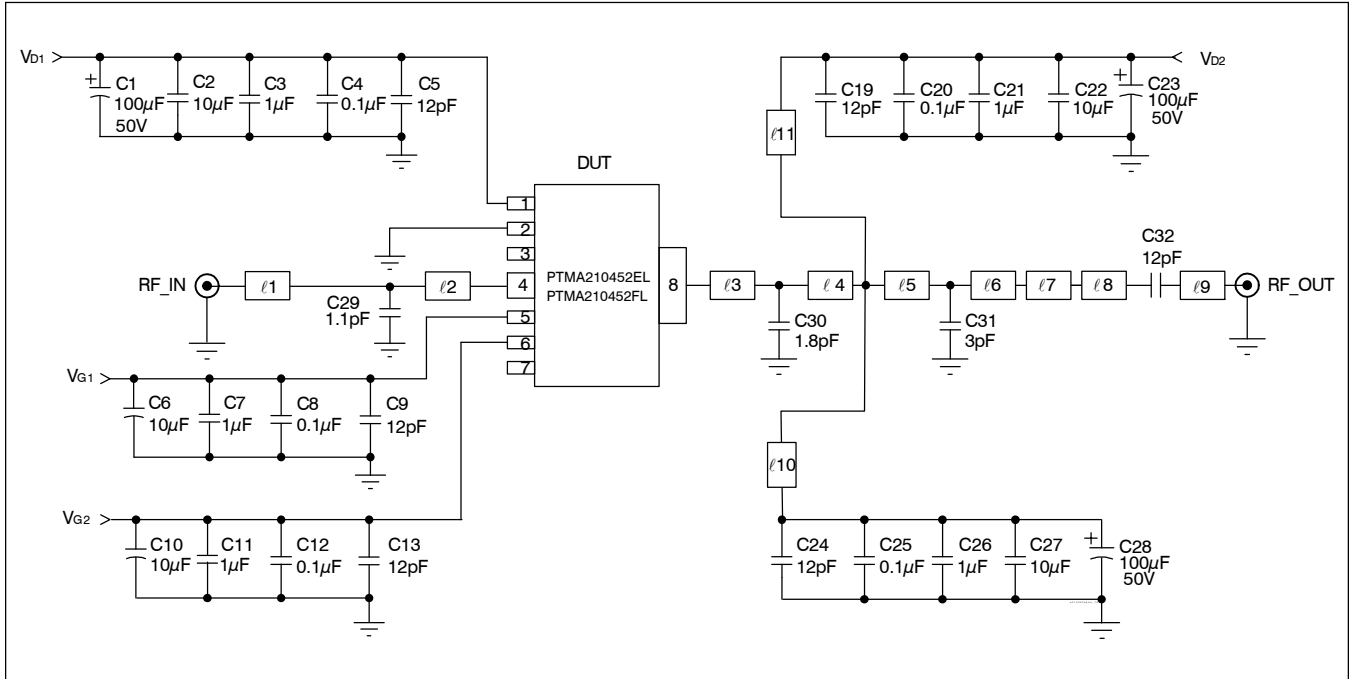
Broadband Circuit Impedance



| Frequency MHz | Z Source W | | Z Load W | |
|------------------|------------|------|----------|------|
| | R | jX | R | jX |
| 1900 | 25.2 | 20.4 | 8.8 | 12.2 |
| 2110 | 26.1 | 27.8 | 6.1 | 16.5 |
| 2140 | 26.2 | 28.9 | 5.9 | 17.1 |
| 2170 | 26.5 | 30.3 | 5.6 | 17.8 |
| 2200 | 26.6 | 5.2 | 18.6 | |



Reference Circuit — for evaluation only



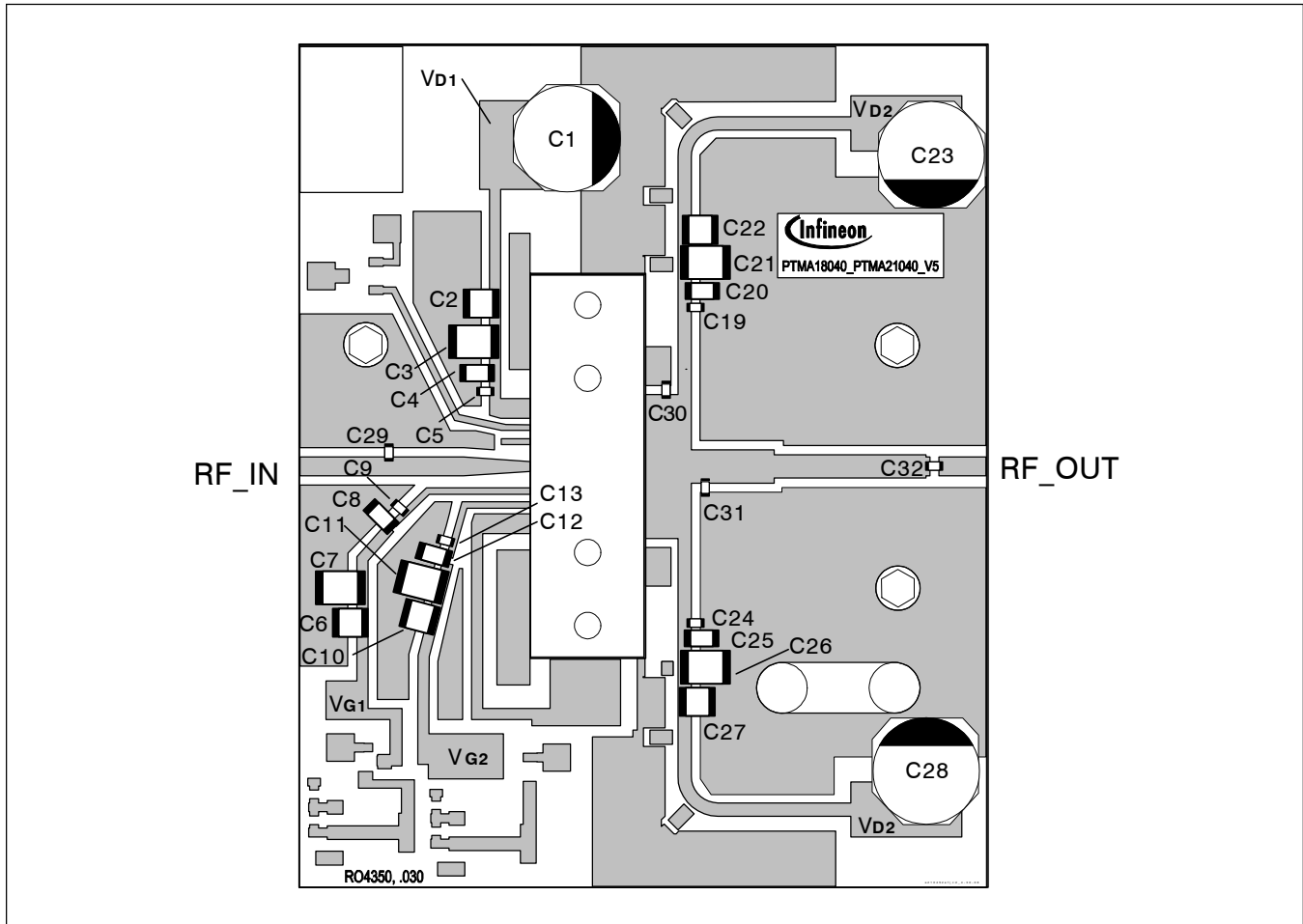
Reference circuit schematic for $f = 2140$ MHz

Circuit Assembly Information

| | | |
|-----|--|----------------------------|
| DUT | PTMA210452EL or PTMA210452FL | LDMOS IC |
| PCB | 0.76 mm [.030"] thick, $\epsilon_r = 3.48$ | Rogers RO4350 1 oz. copper |

| Microstrip | Electrical Characteristics at 2140 MHz | Dimensions: L x W (mm) | Dimensions: L x W (in.) |
|------------------|--|------------------------|-------------------------|
| l_1 | 0.129λ , 49.7 Ω | 11.00 x 1.70 | 0.433 x 0.067 |
| l_2 | 0.114λ , 49.7 Ω | 9.68 x 1.70 | 0.381 x 0.067 |
| l_3 | 0.040λ , 10.4 Ω | 3.10 x 13.00 | 0.122 x 0.512 |
| l_4 | 0.013λ , 10.4 Ω | 1.02 x 13.00 | 0.039 x 0.512 |
| l_5 | 0.024λ , 34.1 Ω | 2.01 x 3.00 | 0.079 x 0.118 |
| l_6 | 0.066λ , 34.1 Ω | 5.46 x 3.00 | 0.215 x 0.118 |
| l_7 | 0.162λ , 43.4 Ω | 13.67 x 2.11 | 0.538 x 0.083 |
| l_8 | 0.004λ , 49.7 Ω | 0.38 x 1.70 | 0.015 x 0.067 |
| l_9 | 0.050λ , 49.7 Ω | 4.24 x 1.70 | 0.167 x 0.067 |
| l_{10}, l_{11} | 0.128λ , 61.2 Ω | 11.00 x 1.19 | 0.433 x 0.047 |

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

| Component | Description | Suggested Manufacturer | P/N or Comment |
|----------------------------|--|------------------------|--------------------|
| C1, C23, C28 | Electrolytic capacitor 100 μ F, 50 V | Digi-Key | PCE3718CT-ND |
| C2, C6, C10, C22, C27 | Ceramic capacitor 10 μ F | Murata | GRM422Y5V106Z050AL |
| C3, C7, C11, C21, C26 | Ceramic capacitor 1 μ F | Digi-Key | 445-1411-2-ND |
| C4, C8, C12, C20, C25 | Capacitor, 0.1 μ F | Digi-Key | 399-1267-2-ND |
| C5, C9, C13, C19, C24, C32 | Ceramic capacitor 12 pF | ATC | 600S120JT |
| C29 | Ceramic capacitor 1.1 pF | ATC | 600S1R1BT |
| C30 | Ceramic capacitor 1.8 pF | ATC | 600S1R8BT |
| C31 | Ceramic capacitor 3 pF | ATC | 600S3R0BT |
| Not used | C14, C15, C16, C17, C18 | | |

*Gerber Files for this circuit available on request

Package Specifications

Package H-33265-8 Outline

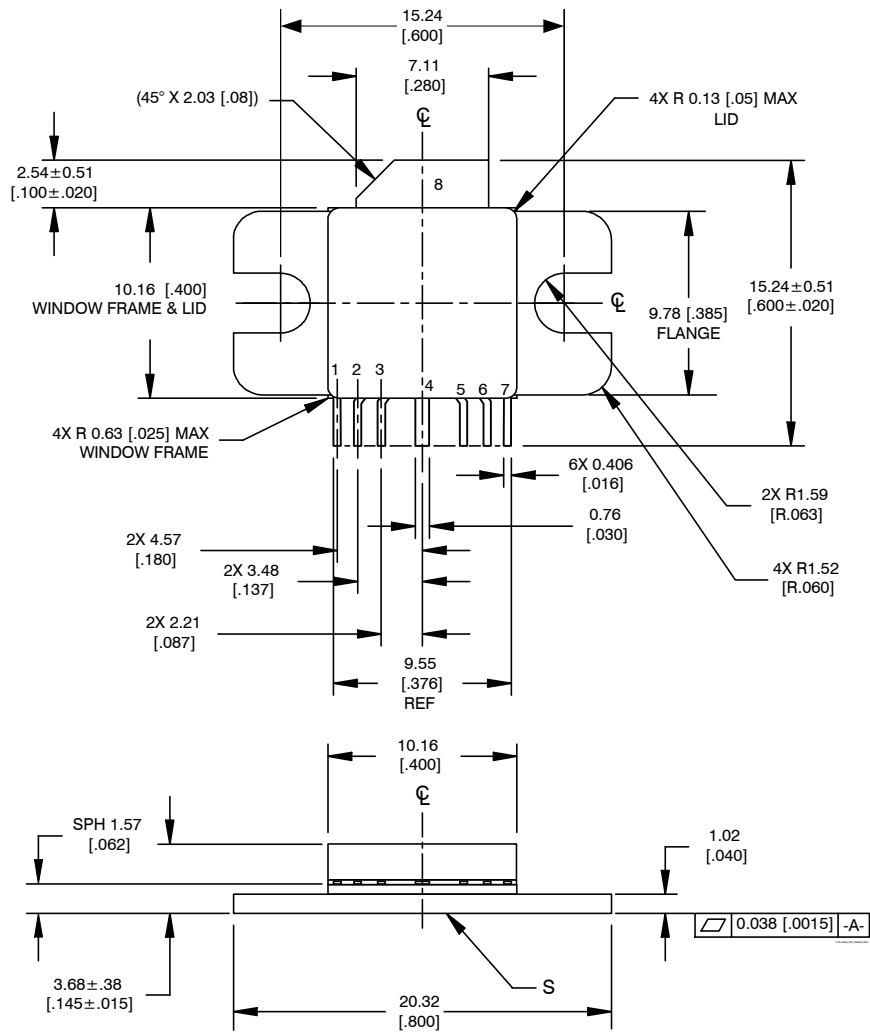


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Pins: S = source; see page 10 for complete list and diagram.
3. Lead thickness: 0.127 ± 0.025 [0.005 ± 0.001].
4. Gold plating less than 0.25 micron [10 microinch].
5. All tolerances ± 0.127 [0.005] unless specified otherwise.
6. Primary dimensions are inches, alternate dimensions are mm.

Package Specifications (cont.)

Package H-34265-8 Outline

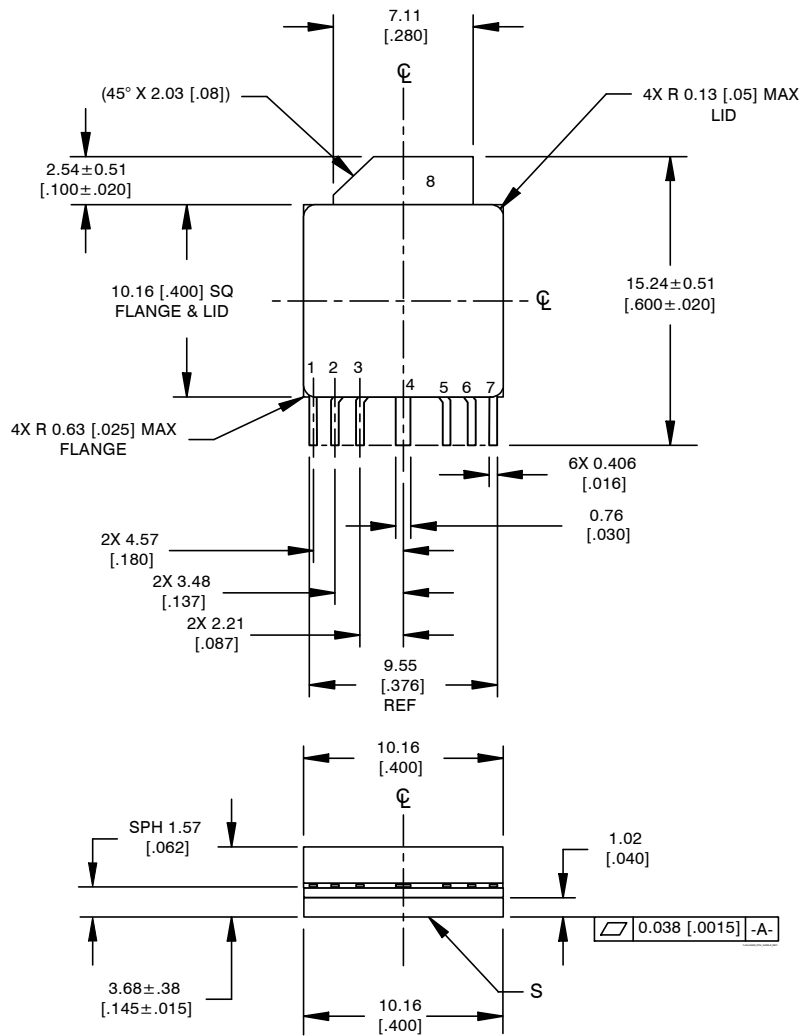
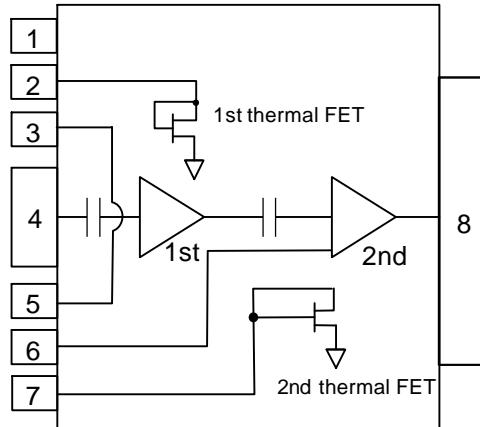


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6. Primary dimensions are inches, alternate dimensions are mm.

Package Specifications (cont.)

Package H-3X265-8 Pinout



| Pin # | Function |
|------------|-------------------------------|
| S - flange | Source (see Package Outlines) |
| 1 | Drain 1 |
| 2 | 1st stage thermal FET |
| 3 | Gate 1 |
| 4 | RF In |
| 5 | Gate 1 |
| 6 | Gate 2 |
| 7 | 2nd stage thermal FET |
| 8 | RF Out |

Find the latest and most complete information about products and packaging at the Infineon Internet page <http://www.infineon.com/rfpower>

Revision History: 2008-07-10

Data Sheet

Previous Version: 2008-05-01, Data Sheet

| Page | Subjects (major changes since last revision) |
|------|--|
| 4, 5 | Performance curves: duplicate graphs removed or combined; Gate – Source Voltage vs. Temperature graph added. |
| | |
| | |
| | |

We Listen to Your Comments

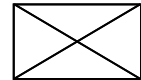
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